CURRICULUM VITAE

Ms. SHITAL MADHUKAR DHAT
(Mrs. Shital Sachin Pathak)
Education Qualification: M.E. (Electronics & Telecommunication)
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PermanentAddress:-

JB-9, Tirupati Supreme Enclave, Jalan Nagar, Near Railway Station,

Chh Sambhajnagar, Maharashtra.

Educational Degrees

M. E.	Master of Engineering (Electronics and Communication Engineering) from Dr. BAM University, MIT College of Engineering, Chh. SambhajiNagar in **Distinction** with CGPA = **8.26** in year 2016
B. E.	Bachelor of Engineering (Electronics and Telecommunication) from Dr. BAM University MBES's College of Engineering, Ambajogai Dist: Beed, Maharashtra in **First Class** with **65.53%** in year 2003
HSC	"Yogeshwari college", Ambajogai Dist : Beed, Maharashtra in **Distinction** with **80.83%** in year 1999
SSC	"Smt. Godavaribai Kunkulol Yogeshwari Kanya Shala Ambajogai, Dist- Beed, Maharashtra in **Distinction** with **82.93%** in year 1997

Positions Held

- Working as an Assistant Professor in MIT (ECE) Chh. Sambhajinagar from 24/06/24 to till date.
- Worked in private coaching classes from Nov 2017 up to March 2019
- Worked as support engineer in Perfect Solutions (I) Pvt LTD, Thane (W) from 08th Jan 2010 to 31st March 2014
- Worked as lecturer in Mucchalla Polytechnic college, Thane (W) from 08th July 2008 to 15th December 2011
- Worked as Dr. BAM university UGC approved lecturer in N.H. college

of Engineering, Parli-Vaijnath Dist: Beed from 16th April 2004 to 31th May 2008

- ❖ Worked as trainee electronics engineer at "Videocon Appliances Ltd", Chitegaon, Chh. Sambhaji Nagar, Aurangabad from 08st Oct 2003 to 13st April 2004

Subject Taught

- Electronics Design Technology
- Communication Engineering
- Sensors and Signal Conditioning
- Digital Signal Processing
- Digital Systems
- Electronics Devices and Circuits
- Opto-Electronics
- Basic Electrical

Project Details

Dissertation in ME

Congestion Control using Received Signal Strength in AODV for MANETs

CCAODV new cross layer design-based algorithm is used to avoid link break in MANETs. The cross-layer design approach was tested by Ns2.35 simulator and its performance over AODV was found to be better.

Project in BE

Programmable Power Converter

Basic Circuit of cycloconverter using Centre tap transformer is used. 8085 microprocessors with 8255 as PPI is used in this project. Without changing hardware this project provides AC and DC power control in different modes.

Software Skills

Languages: - C, Python

Software: - Ms- Word, Excel, PowerPoint, NS2, Matlab

Operating Systems: - Microsoft word, Linux, Ubuntu.

Papers Published

Sr. N0	Title/subjectofJournal	Nameofthe Author	Nameofthe Journal	Volume&Issue	Yearof Publication
1	"Congestion Control Using Signal Strength in MANET: Review Paper"	Shital M Dhat, Dr. Abhilasha Mishra, Mazher Khan	InternationalJournalon Modern Trends in Engineering, Science and Technology, IJRITCC	Vol 4, pp 380-383	2016
2	"Cross Layer Design Approach for Congestion Control in MANETs"	Mazher Khan, Shital M Dhat, Dr. Sayyad Ajij D	IEEE conference on Advances in Electronics, Communication and Computer TechnologyICAECCT	Vol 6, pp 247-248	2016

Responsibilities

- Test coordinator for ISE exams.
- Team member in central admission committee.
- Lab-Incharge for Power Electronics lab.
- Class-coordinator.
- Internal verification committee member of ISE exams.
- NPTEL departmental coordinator.
- Supervise student projects, field trips and appropriate placements.
- Plan and organize guest lecture from eminent people in academics/ industry or research.
- Initiate co-curricular and extra-curricular activities for student development. Plan and conduct the events and activities allocated.
- Motivate the students for participating in technical events, project competitions,
- Worked as an examination sub-coordinator for conducting exams.
- Develop innovative approaches to course design and deliver a range of courses at various levels including preparation of course plan, effective conduction of lectures and maintain attendance.

Workshop Attended

- FDP on 'IoT Integration with Embedded System', from 6 th January to 11th January 2025, ATAL.

- Online FDP ‘Inculcating Universal Human values in Technical Education’ by AICTE from 23rd December to 27 th December 2024.
- FDP on ‘Innovative Teaching Pedagogy and Skills Component of NEP’, 9th December 2024 at Chh. Sambhajinagar.
- FDP on ‘The Art and Science of Generative AI’, from 8th July to 12 July 2024 held at MIT, Chh. Sambhajinagar.
- FDP on ‘C Programming’, from 27th June to 3rd July 2024 at MIT Chh. Sambhajinagar.
- ‘WSN Fundamentals and Protocol Design using NS-2 and NS-3’, 23rd and 24th January 2016, Two days state level STTP at Sinhgad Institute of Technology, Lonavala, Maharashtra.
- ‘Advances in Biomedical Instrumentation’, from 01stJan 2006 to 3rd Jan. 2006, SGGSIOE and T, Nanded, Maharashtra.
- ‘C-DSP-VLSI Design’, form 11th Apr. 2005 to 16 Apr. 2005, N.H. COE, Parli-V, Dist-Beed, Maharashtra.

Declaration

I can do the job with great sense of responsibility and always try to make a positive contribution and efforts to prove myself as an asset to the organization.

Place: Chh. Sambhaji Nagar (Aurangabad)

Date:

(Ms.Shital M.Dhat)
Mrs. Shital Sachin Pathak