Resume

Manasi Rajesh Vargantwar
Associate Professor, Department of Electronics and Computer Engineering,
MIT, CSN
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Academic Credentials

Class/ Degree	Specialization	Institution	University	Year	%/CGPA	Class
M.E.	Electronics	Government EngineringCollege, Aurangabad	*Dr. B.A.M.U./ GECA*	*2008*	*78.75*	*First Division with Distinction*
PGDIM		NIT, Nagpur	*Nagpur University/ VRCE, Nagpur*	*1996*	*70.63*	*I Division*
B.E.	Electronics	Walchand Institute of Technology, Aurangabad	*Shivaji University/ WIT, Solapur*	*1994*	*73.47*	*First Class with Distinction*

Key Study Area

Signal Processing, VLSI Design

Membership of Professional Bodies

- Life Member of ISTE (LM-41077)
- Life Member of IETE (M-177604)

Projects Guided

PG Projects Guided: 19

UG Projects Guided: Several

Computer/Software Proficiency

- MATLAB
- VHDL
- Python Programming

Awards, Achievements and Recognition

- Obtained Certificate of appreciation for being the organizer on behalf of MIT for Analog Maker competition 2014 conducted by Texas Instruments India University Program in association with Edgate Technologies and MIT
- Awarded with "Women's achievement award" 2017" given by Arya Vaishya Lions Aurangabad

Academic Experience

Sr. No.	Organization	Designation	From	To
1	Maharashtra Institute of Technology, Chh. Sambhajinagar	**Associate Professor**	**July 2022**	**Till Date**
2	Marathwada Institute of Technology , Aurangabad	Associate Professor, Department of ETC	24. 06.2009	June 2022
3	Maharashtra Institute of Technology , Aurangabad	Assistant Professor, Department of ETC	01.07.2008	18.06.2009
4	M. I. T. Polytechnic, Aurangabad	Lecturer, Department of ETC	10.07. 99	30.06.08
5	Marathwada Institute of Technology , Aurangabad	Lecturer, Department of ETC	06.08.98	17.06.99

Industry Experience

- **Name of the Company: Aska Equipments Pvt. Ltd.**

  Designation: System Engineer (Hardware/ Software)

  Period: From 01.08.95 to 31.05.97

- **Name of the Company: Diglin Industries**

  Designation: Graduate Trainee Engineer

  Period: From 09.03.95 to 08.07.95

Work Experience

- Developed DSP/ VLSI Lab
- Worked as Exam Control Cell Incharge
- Central Term Work Coordinator
- Central Time Table Incharge
- NIRF, AICTE etc. Coordinator, Admission Committee Member

Publications, FDP, STTPs and Courses Taught

- Developed DSP/ VLSI Lab
- Arranged STTPs, Workshops
- Attended FDPs, STTPs
- Taught several UG / PG Courses

Date: 21.04.2025

Place: Chhatrapati Sambhaji Nagar