

## Curriculum Vitae

**Name: Ms.P.P.Patil**



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Dist. –Aurangabad.

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**Mobile: 9028384800**

**Date of Birth: 4<sup>th</sup> July 1987**

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### Academic Credentials

Class/ Degree	Specialization	Institution	University	Year	%/ CGPA	Class
M.E./ M. Tech.	Electronics	Government college of Engineering Aurangabad	Dr.B.A.M. University, Aurangabad	2011	8.34	<i>Distinction</i>
B.E./B.Tech.	ETC	Government college of Engineering Jalgaon	North Maharashtra University Jalgaon	2008	70.85 %	<i>Distinction</i>

**M. Tech. Project:** DWT based image compression using VLSI

**Key Research Areas: Image Processing**

## Experience

Sr. No.	Organization	Post	From	To	No. of Years
1	Maharashtra Institute of Technology ,Aurangabad	Assistant Professor	1 <sup>st</sup> August 2012	to till date	7 years 6 months
2	P.E.S. College of Engineering	Visiting Lecturer	Jan 2010 to April 2010		4 Months
3	Bhambhori College of Engineering,Jalgaon	Lecturer	July 2008 to April 2009		10 Months

## List of Courses Taught/Teaching at UG level –

1. Analog Electronics
2. Electronics Measurement
3. Basic Electronics
4. Electronics Devices and Circuits
5. Integrated Circuits and Applications
6. HSAD

## Membership of Professional Bodies

1. Life Member of ISTE  
Membership number: LM 107493

## Computer/Software Proficiency

1. C, C++. MS Windows, MS Office (MS Word, MS Excel, and MS Power Point) & Internet ,MS Office Front page, Photoshop, Flash.
2. Hardware & Networking

## Seminar/Workshop/Industrial Training/STTP//FDP/CEP/Conference Attended

1. Attended a Five days workshop on “System Design Using FPGA(SDF-2013) “ at Government college of Engineering Aurangabad from 24<sup>th</sup> June -28<sup>th</sup> June 2013.
2. Attended a One Day Faculty Development Programme on “Professional English Communication Skills” at Maharashtra Institute of Technology Aurangabad on 17<sup>th</sup> Jan 2015.
3. Attended a One Day workshop on “Research Methodology “ at P.E.S. College of Engineering Aurangabad on 20<sup>th</sup> August 2016.
4. Attended One week FDP on “Data Sciences” Funded by MHRD at Maharashtra Institute of Technology, Aurangabad.

### **Seminar/Workshop/Industrial Training/STTP//FDP/CEP/Conference organized**

1. Organized Two Days National Level Workshop on “Research Methodology” at Maharashtra Institute of Technology Aurangabad from 13<sup>th</sup> March 2015 to 14<sup>th</sup> March 2015.
2. Organized Four Days National Level Workshop on “Matlab, Simulink and Low Cost Design using Signal & Image Processing Toolbox” at Maharashtra Institute of Technology Aurangabad during 16<sup>th</sup> December 2015 to 19<sup>th</sup> December 2015.
3. Organized One Day Hands-on-Training Program on “Need of Electronics in Industry for Electrical and ETC Engineers” For Second Year Student at Maharashtra Institute Of Technology Aurangabad on 20<sup>th</sup> Feb 2017
4. Organized 1<sup>st</sup> International Conference on “Digital Signal and Image Processing” at Maharashtra Institute of Technology ,Aurangabad on 7<sup>th</sup> and 8<sup>th</sup> March 2017.
5. Organized IEEE conference AEMC 17 at Maharashtra Institute of Technology, Aurangabad.

### **NPTEL Certification**

Start Date	End Date	Duration (in Weeks)	Course Name	Marks (Out of 100)	Performance
March	April	4	TALE	75	

### **Awards, Achievements and Recognition**

Selected as Best Paper Presenter and Got First Prize at Converges'11, A National Level Technical Symposium, organized by R.C.Patel Institute of Technology Shirpur .

Date: 28/02/2020

Place: Aurangabad